Notice of Allowability	Application No.	Applicant(s)	
	10/771,565	JUENGLING ET AL.	
	Examiner	Art Unit	
	William C. Vesperman	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *2/4/2004*.

2. ☒ The allowed claim(s) is/are *1-8*.

3. ☒ The drawings filed on *04 February 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 5/7/2004
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. This action is in response to applicant's filing of 2/4/2004.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with John Reed on 6/18/2004.

Please replace Claims 1, 5 and 6 with revised Claims 1, 5 and 6 as shown below.

1. A reticle used to make memory cells, said reticle comprising:

at least one generally planar surface defining a plurality of lead line cutouts and a plurality of fill pattern cutouts therein, said plurality of fill pattern cutouts interspersed between said plurality lead line cutouts and spaced apart from each of said plurality of lead line cutouts by an amount sufficient to avoid capacitive communication between a metal lead line and a metal fill pattern formed on a memory cell by said reticle, wherein said plurality of lead line and fill pattern cutouts are disposed in an array within a surface of said reticle such that a substantially continuous straight-edged perifery around said array is defined by at least one of said lead line and fill pattern cutouts, and no portion of any of said fill pattern cutouts within said array extends laterally beyond said periphery; and

a grid defined by at least a portion of said surface, said grid comprising an interconnected series of spaces between each adjacent said plurality of lead line and fill pattern cutouts such that a lateral distance defining the width of any one

of said series of spaces is substantially equal to that of any other of said series of spaces within said grid, the longest linear dimension between each of said series of spaces is no longer than the longest dimension of any of said plurality of fill pattern cutouts and no intersection defined by a crossing between any two of said interconnected series of spaces includes uninterrupted linear dimensions.

5. A semiconductor fabrication system comprising:

a photoresist application mechanism to deposit photoresist onto a semiconductor substrate;

an electromagnetic radiation source to illuminate at least a portion of said photoresist;

a solvent dispensing mechanism to wash away unexposed photoresist;

an etching mechanism to selectively remove at least one layer of insulative coating; and

a reticle with a generally planar body that occupies first and second substantially orthogonal dimensions; said reticle comprising:

a first segment of said generally planar body defined by a plurality of cutouts therethrough, said cutouts adapted to define topographic peaks on a semiconductor, where said cutouts are shaped to further define at least one lead line and a plurality of dummy patterns spaced apart from one another;

a second segment of said generally planar body comprising the remainder thereof such that a pattern formed by said remainder extends in said first and second substantially orthogonal dimensions, said remainder adapted to define a plurality of interpeak valleys on said semiconductor;

a geometrically simple array defined by said plurality of cutouts, wherein:

a substantially continuous straight-edged periphery around said array is defined by at least one of

said lead line and dummy pattern cutouts of said first segment; and

no portion of any of said plurality of said dummy patterns within said first segment extends laterally beyond said periphery of said array; and

a grid defined by at least a part of said second segment such that the longest linear dimension in the portion of said second segment bounded by said periphery is no longer than the longest linear dimension of any part of said first segment and no intersection formed in said second segment includes uninterrupted linear dimensions.

6. A method for fabricating a reticle, said method comprising:

producing a plurality of lead line cutouts in a reticle body;

producing a plurality of fill pattern cutouts interspersed between said plurality lead line cutouts, and spaced apart from each of said plurality of lead line cutouts by an amount sufficient to avoid capacitive communication between a metal lead line and a metal fill pattern formed on a memory cell by said reticle, wherein said plurality of lead line and fill pattern cutouts are disposed within a surface of said reticle such that a substantially continuous straight-edged periphery around said array is defined by at least one of said lead line and fill pattern cutouts, and no portion of any of said plurality of fill pattern cutouts extends laterally beyond said periphery; and

forming a grid comprising an interconnected series of spaces between each adjacent said plurality of lead line and fill pattern cutouts, where a lateral distance defining a width of any one of said series of spaces is substantially equal to that of any other of said series of spaces within said grid, such that the longest linear dimension between each of said series of spaces is no longer than

the longest dimension of any of said plurality of fill pattern cutouts and no intersection defined by a crossing between any two of said interconnected series of spaces includes uninterrupted linear dimensions.

Reasons For Allowance

3. Claims 1 – 8 are allowed.

4. The following is an examiner's statement of reasons for allowance.

Harvey (US 5,854,125) discloses (Figures 2d, 3a – 3c) a method of fabricating a semiconductor wafer, comprising: providing a generally planar semiconductor wafer substrate such that the substrate is defined by substantially orthogonal first and second in-plane dimensions, defining a topographic layer of conductive lead line material such that said topographic layer projects onto the substrate to occupy at least a portion of the substantially orthogonal first and second in-plane dimensions; depositing at least one topographic layer of conductive lead line material on the substrate, depositing a plurality of topographic fill patterns adjacent either the topographic layer of conductive lead line material or another of the plurality of topographic fill patterns such that spaces defined there between possess substantially equal width as any other space and depositing a planarization layer over the substrate such that it is disposed at least within the grid and laterally surrounds the at least one topographic layer of conductive lead line material and the plurality of topographic fill patterns.

The prior art does not teach or fairly suggest, in combination with the other claimed limitations, a reticle comprising: at least one generally planar surface

defining a plurality of lead line cutouts and a plurality of fill pattern cutouts therein, said plurality of fill pattern cutouts interspersed between said plurality lead line cutouts and spaced apart from each of said plurality of lead line cutouts by an amount sufficient to avoid capacitive communication between a metal lead line and a metal fill pattern formed on a memory cell by said reticle, wherein said plurality of lead line and fill pattern cutouts are disposed in an array within a surface of said reticle such that a substantially continuous straight-edged perifery around said array is defined by at least one of said lead line and fill pattern cutouts, and no portion of any of said fill pattern cutouts within said array extends laterally beyond said periphery; and a grid defined by at least a portion of said surface, said grid comprising an interconnected series of spaces between each adjacent said plurality of lead line and fill pattern cutouts such that a lateral distance defining the width of any one of said series of spaces is substantially equal to that of any other of said series of spaces within said grid, the longest linear dimension between each of said series of spaces is no longer than the longest dimension of any of said plurality of fill pattern cutouts and no intersection defined by a crossing between any two of said interconnected series of spaces includes uninterrupted linear dimensions.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled " Comments on Statement of Reasons for Allowance".

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Takizawa (US 6,504,254) teaches a semiconductor device with dummy wiring layers.

Chen et al. (US 6,178,853 B1) teaches a method of designing active patterns with a shifted dummy pattern.

Gabriel et al. (US 5,861,342) teaches a method of improving the planarity of spin on glass layers.

Findley et al. (US 5,763,955) teaches integrated filled layers for integrated circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William C. Vesperman whose telephone number is 571-272-1701. The examiner can normally be reached on Mon. - Fri., 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl White, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Art Unit 2813

June 21, 2004

Tuan H. Nguyen

Tuan H. Nguyen
Primary Examiner